EXHIBIT 21

FILED UNDER SEAL

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC.,	)	
	)	
Plaintiff,	)	
	)	
vs.	)	Case No.
	)	2:22-cv-203-JRG
MICRON TECHNOLOGY, INC.,	)	
MICRON SEMICONDUCTOR	)	
PRODUCTS, INC., and MICRON	)	
TECHNOLOGY TEXAS, LLC,	)	
	)	
Defendants.	)	
	)	

REMOTE VIDEOTAPED DEPOSITION
OF
JOHN BENTLEY HALBERT, III
Saturday, September 30, 2023
Castiglione Falletto, Italy

Reported by: B. Suzanne Hull, CSR No. 13495

APPEARANCES

For Plaintiff: Irell & Manella, LLP
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The Videographer: David West

I N D E X

E X H I B I T S

EXHIBITS (Continued)

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EXHIBITS (Continued)

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EXHIBITS (Continued)

EXHIBITS (Continued)

Castiglione Falletto, Italy
Saturday, September 30, 2023; 4:06 p.m.
Villa Roma 29

THE VIDEOGRAPHER: Good afternoon. We are on the record. 16:06:04
The time is 4:06 p.m. That is 16:06:05
Central European Time. 16:06:12
The date today, September 30th, 2023. 16:06:14
Please note that this deposition is being 16:06:18
conducted virtually.
Quality of recording depends on the quality
of camera and Internet connection of participants.
What is seen from the witness and heard on
screen is what will be recorded.
Audio and video recording will continue to
take place unless all parties agree to go off the
record.
This is media unit one of the video-recorded 16:06:36
deposition of John Halbert taken by counsel for 16:06:40
plaintiff in the matter of Netlist, Inc., versus 16:06:44
Micron Technology, Inc., et al., filed in 16:06:49
United States District Court, for the Eastern 16:06:51
District of Texas, Marshall Division, Case Number 16:06:54
2:22-cv-203-JRG. 16:06:56

The deposition is being conducted remotely 16:06:58
using virtual technology. 16:07:04
My name is David West. I am the 16:07:05
videographer. The court reporter is Suzanne Hull. 16:07:07
We represent Veritext Legal Solutions. 16:07:09
I am not related to any party in this 16:07:11
action, nor am I financially interested in the 16:07:14
outcome. 16:07:17
If there are any objections to proceeding, 16:07:17
please state them at the time of your appearance. 16:07:20
Counsel will now state their appearances and 16:07:22
affiliations for the record, beginning with the 16:07:25
noticing attorney. 16:07:28
MS. ZHONG: Annita Zhong, from 16:07:28
Irell & Manella, representing the plaintiff, Netlist, 16:07:30
Inc. 16:07:34
MR. KRISHNAN: Vivek Krishnan, of 16:07:35
Winston & Strawn, on behalf of Micron and the 16:07:37
witness. 16:07:42
THE VIDEOGRAPHER: Thank you. 16:07:43
The court reporter may now swear the witness 16:07:44
in, and we will continue. 16:07:47
THE REPORTER: Raise your right hand, 16:07:49
please, sir. 16:07:51
Do you solemnly swear or affirm that the 16:07:52

MR. KRISHNAN: Objection. Form. 19:12:31
THE WITNESS: Yeah. 19:12:34
You could say that wire bond was the most 19:12:35
common. 19:12:38
BY MS. ZHONG: 19:12:38
Q. Okay. At least in 2009 to 2010 time period 19:12:38
the wire bond connection is -- was the most common 19:12:44
for the dual die package and the quad die package; is 19:12:48
that correct? 19:12:51
MR. KRISHNAN: Objection. Form. 19:12:52
THE WITNESS: Yes. 19:12:53
Wire bond was probably the most common. 19:12:55
BY MS. ZHONG: 19:12:55
Q. Okay. So for those wire-bonded packages, 19:12:58
would the electrical and the mechanical con- -- would 19:13:03
the electrical connection for an upper die go through 19:13:06
the lower die? 19:13:13
MR. KRISHNAN: Objection. Form. 19:13:15
THE WITNESS: The fact that it is wire bond 19:13:17
would say that the wires connecting the upper die 19:13:21
would go down to the package. 19:13:25
BY MS. ZHONG: 19:13:27
Q. Okay. Was -- without going through the 19:13:27
lower die? 19:13:29
MR. KRISHNAN: Objection. Form. 19:13:30

THE WITNESS: Correct. 19:13:34
BY MS. ZHONG: 19:13:36
Q. Okay. And you mentioned earlier that there 19:13:36
were connections -- there were manufacturers that 19:13:38
connect the die along the outside edge of the die. 19:13:46
Were those down in the 2009 to 2010 period? 19:13:51
MR. KRISHNAN: Objection. Form. 19:13:58
THE WITNESS: That is a good question. 19:13:59
There was -- 19:14:00
BY MS. ZHONG: 19:14:00
Q. I don't -- not when was it done? When did 19:14:00
they start to do it? Maybe that is a better 19:14:05
question. 19:14:07
A. I don't remember. Everything kind of blurs 19:14:08
together back then. There were a lot of different 19:14:10
technologies being proposed and produced to create 19:14:13
a better stack. 19:14:18
Q. Okay. 19:14:19
A. So whether it was 2009-'10, I don't 19:14:19
remember. Or earlier. 19:14:24
Q. Do you know whether it is -- it was done by 19:14:24
2011-2012? 19:14:27
MR. KRISHNAN: Objection. Form. 19:14:34
THE WITNESS: My guess it probably was -- 19:14:35
///

BY MS. ZHONG: 19:14:38
Q. Okay. 19:14:38
A. -- in that time frame. 19:14:38
Q. But you don't know for sure? 19:14:40
A. No. 19:14:45
Because it has been too long. 19:14:45
Q. Okay. Can you use a DRAM circuit in DDRs, 19:14:48
LRDDRs for HBM? 19:15:29
MR. KRISHNAN: Objection. Form. 19:15:33
THE WITNESS: What -- what are you asking? 19:15:36
BY MS. ZHONG: 19:15:38
Q. Okay. 19:15:38
A. You are mixing a bunch of terms together. 19:15:39
Q. Okay. Can you use a DRAM circuit in DDR2? 19:15:41
A. What do you define as DRAM circuits? 19:15:51
Q. What is your understanding of the term DRAM 19:15:55
circuit? 19:15:57
A. I think it -- you are the one asking the 19:15:58
question. You are -- you need to clarify what your 19:16:01
question is. 19:16:04
Q. Okay. Is there -- is the word DRAM circuit 19:16:05
a term of art? 19:16:08
A. A term of the art? No. 19:16:10
Q. So what is your understanding of DRAM 19:16:13
circuit? 19:16:18

A. So a DRAM circuit -- 19:16:19
MR. KRISHNAN: Objection. Form. 19:16:22
THE WITNESS: From a design point of view, 19:16:23
a DRAM circuit would be anything outside of the cell 19:16:26
array that only contains memory cells; so a DRAM 19:16:29
circuit would include the sense sound, the column 19:16:34
decoder, the row decoder. And maybe even the 19:16:38
secondary sense amps along the I/O are all DRAM 19:16:42
circuits that are only used in DRAMs. 19:16:47
BY MS. ZHONG: 19:17:06
Q. Are the same DRAM circuits used for 19:17:07
different types of DRAM devices? 19:17:10
A. So all -- well, kind of put that in quotes. 19:17:15
Let's say 99 percent of anything that has DRAM cells 19:17:21
will have DRAM circuits included. Like I mentioned, 19:17:28
sense amps, column decoders, row decoders, secondary 19:17:34
sense amps. 19:17:42
Q. Okay. What about circuits for IEEE testing? 19:17:43
A. Uh-huh. 19:17:56
Q. Do they have -- are those DRAM circuits? 19:17:58
MR. KRISHNAN: Objection. Form. 19:18:04
THE WITNESS: That is kind of a goofy 19:18:06
question. 19:18:12
BY MS. ZHONG: 19:18:12
Q. Okay. 19:18:12

A. I mean, it is like trying to mix apples and oranges. 19:18:13 19:18:17
Q. Okay. 19:18:18
A. So you are saying -- are you asking if JTAG is used on DRAMs? 19:18:18 19:18:25
Q. JTAG? J-T-A-G? 19:18:28
A. Yeah. 19:18:39
Q. Yes. 19:18:39
So my understanding is that HBM has pretty advanced testing capabilities in them. 19:18:39 19:18:45
Is that your understanding as well? 19:18:48
A. Yes. 19:18:51
MR. KRISHNAN: Objection to form. 19:18:51
BY MS. ZHONG: 19:18:53
Q. Okay. So -- so there has got to be testing circuits in the HBM packages; correct? 19:18:53 19:18:58
MR. KRISHNAN: Objection to form. 19:19:03
THE WITNESS: There are testing circuits -- yeah. 19:19:04 19:19:04
There are testing circuits in HBM packages. They are also testing circuits on each die in the stack. 19:19:05 19:19:10 19:19:14
BY MS. ZHONG: 19:19:15
Q. Okay. So are those testing circuits what you call -- what -- what you would refer to as DRAM 19:19:15 19:19:18

circuits? 19:19:22
MR. KRISHNAN: Objection. Form. 19:19:24
THE WITNESS: So, again, you are, kind of -- you are trying to twist terms around, which makes it very difficult to answer the question. If your question is are there common testing circuits between the die and the HBM stack and in the base die and in monolithic -- i.e., DDR3 or DDR4 -- the answer is yes. 19:19:25 19:19:38 19:19:42 19:19:45 19:19:51 19:19:58 19:20:06
BY MS. ZHONG: 19:20:07
Q. Are there unique testing circuits for the HBM products? 19:20:12 19:20:16
MR. KRISHNAN: Objection. Form. 19:20:20
THE WITNESS: Hmmm. It depends on which testing circuits we're talking about. Some are common between monolithic DRAMs, DDR3 and HBM, especially at the die test level. 19:20:21 19:20:25 19:20:31 19:20:43
BY MS. ZHONG: 19:20:45
Q. Uh-huh. 19:20:45
A. And so the die and the stack -- in the HBM stack have to have I/O circuits that allow the test machine to test all of the DRAM cells. And because there are so many cells, there are test circuits that test many cells in parallel. This is a common method used in testing DRAMs, whether they are in the HBM 19:20:46 19:20:49 19:20:54 19:20:58 19:21:04 19:21:09

stack or they are a mono die. 19:21:13
Q. Okay. But are there testing circuits unique to the HBM products? 19:21:17 19:21:24
MR. KRISHNAN: Objection. Form. 19:21:25
THE WITNESS: Yes. 19:21:27
So there is an IEEE 1500 bus on the base die. There is also -- there is probably other -- there is testing circuits for checking the connection between the base die and the vols in the package; so those -- those would be unique to HBM. But I believe there are other die that have -- or other standards that have copied that for DRAM that have many outputs. 19:21:38 19:21:43 19:21:49 19:21:53 19:21:59 19:22:07 19:22:10 19:22:15
BY MS. ZHONG: 19:22:15
Q. Okay. So let's stay on that. 19:22:16
Is the IEEE testing circuits on both the logic die, as well as the DRAM device die? 19:22:20 19:22:27
A. No. 19:22:31
Q. So there are no corresponding circuits on the memory die? 19:22:31 19:22:41
A. For an IEEE 1500 bus, no. Because that is used to -- as a method to address the stack once it is all put together. 19:22:42 19:22:49 19:22:54
Q. Are you saying the circuit only exists on the logic die but not on the DRAM die? 19:22:55 19:23:05

MR. KRISHNAN: Objection. Form. 19:23:09
THE WITNESS: So IEEE 1500 is a testing standard that has lots of functionality to it. JTAG, as I mentioned -- J-T-A-G -- is a simpler method of testing, less robust. It may or may not be included by the memory suppliers on the mono die as a method to reduce the number of connections that they have to make to the die when it is in wafer form; so it could very well be a version of a serial access to the die in the stack. But I can't answer that because that would be a supplier -- and we call it secret sauce. 19:23:10 19:23:15 19:23:27 19:23:30 19:23:38 19:23:44 19:23:47 19:23:52 19:23:59 19:24:02
BY MS. ZHONG: 19:24:09
Q. Okay. So if there is an IEEE 1500 testing circuit on the DRAM die, that would be unique to the HBM DRAM and is absent from monolithic PDRs; is that right? 19:24:10 19:24:16 19:24:23 19:24:31
MR. KRISHNAN: Objection. Form. 19:24:32
THE WITNESS: There is no reason to include -- as I said, IEEE 1500, it is a very robust serial bus access to the -- 19:24:36 19:24:37 19:24:47
BY MS. ZHONG: 19:24:49
Q. Uh-huh. 19:24:49
A. -- die. It is used in other chips, probably CPUs. There is no -- if you have a die that only has, what, sixteen I/Os -- 19:24:50 19:24:54 19:24:58